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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,638	10/04/2006	Tatsuo Sasaoka	P30908	2109

52123 7590 11/13/2008

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EXAMINER	
DIBERNARDO, DAVID J	

ART UNIT	PAPER NUMBER
4136	

NOTIFICATION DATE	DELIVERY MODE
11/13/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/599,638	SASAOKA ET AL.	
	Examiner	Art Unit	
	David J. DiBernardo	4136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/4/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Preliminary Amendment

1. Receipt is acknowledged of the preliminary amendment filed 4 January 2007.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6-9, 11-16, 18-19 and 21-22 rejected under 35 U.S.C. 102(e) as being anticipated by Tong et al. (U.S. Patent No. 6,902,987, from hereinafter "Tong").

Regarding independent claims 1, 13 and 22, Tong discloses surface-treating by controlling at least one of the bonding surfaces to be bonded together so as to have a predetermined roughness (The surface 33 of layer 32 is planarized and smoothed, as shown in step 2 of FIG. 1 and in FIG. 3B. It is noted that the roughness/planarity of surface 33 is exaggerated in FIG. 3A for illustrative purposes. This step may be accomplished using chemical-mechanical polishing. Surface 33 is preferably polished to a roughness of about no more than about 3 nm and preferably no more than about 0.1 nm and be substantially planar. The surface roughness values are typically given as root-mean square (RMS) values. Also, the surface roughness may be given as mean values which are nearly the same as the RMS values; See Col. 5, Lns. 16-26), and

removing a bonding inhibitor substance from the bonding surfaces (After polishing surface 33 is cleaned and dried to remove any residue from the polishing step. Polished surface 33 is preferably then rinsed with a solution; See Col. 5, Lns. 27-30) and attaching a bonding enhancer substance on the bonding surfaces (Alternatively, a post-VSE treatment that activates and terminates the surface with a desired terminating species during the post-VSE process may be used. The desired species further preferably forms a temporary bond to the surface 34 atomic layer, effectively terminating the atomic layer, until a subsequent time that this surface can be brought together with a surface terminated by the same or another bonding species 36 as shown in FIG. 3D. Desired species on the surfaces will further preferably react with each other when they are in sufficiently close proximity allowing chemical bonding between surfaces 34 and 36 at low or room temperature that is enhanced by diffusion or dissociation and diffusion of the reacted desired species away from the bonding interface. The post-VSE process preferably consists of immersion in a solution containing a selected chemical to generate surface reactions that result in terminating the bonding surface 34 with desired species; See Col. 6, Lns. 20-34); and bonding by bringing the bonding surfaces of the two or more objects into contact with each other and bonding them (Two wafers are bonded by aligning them (if necessary) and bringing them together to form a bonding interface. As shown in FIG. 3D, a second wafer 35 has been processed in the manner shown in FIG. 3C to prepare bonding surface 36. The two wafers are brought together by, for example, commercially available wafer bonding equipment (not shown) to initiate bonding interface 37; See Col. 6, Lns. 58-65).

Regarding claims 2 and 14, Tong discloses the bonding method and apparatus wherein the surface-treatment step includes an initial surface cleaning step of removing bonding inhibitor substances that exist on the bonding surfaces (After polishing surface 33 is cleaned and dried to remove any residue from the polishing step. Polished surface 33 is preferably then rinsed with a solution; See Col. 5, Lns. 27-30).

Regarding claims 3 and 15, Tong discloses the bonding method and apparatus wherein each step is performed under the atmospheric pressure (The need to apply voltage, pressure or heat has significantly limited wafer bonding applications because these parameters can damage the materials being wafer bonded, give rise to internal stress and introduce undesirable changes in the devices or materials being bonded. It is thus highly desirable to achieve a strong bond at room temperature by bonding wafers in ambient without any adhesive, external pressure or applied electric field. It is an object of the invention to provide a method for bonding materials at low or room temperature; See Col. 1, Lns. 22-27 and 45-48, Col. 2, Lns. 21-22).

Regarding claims 4 and 16, Tong discloses the bonding method and apparatus wherein, when the bonding surface has a surface roughness that is inappropriate for the materials to serve as a bonding surface, controlling of the surface roughness include a step of processing and controlling the bonding surfaces to have an appropriate surface roughness (The bonding surface may also be etched prior to polishing to improve the planarity and/or surface roughness. The etching can be effective to remove high spots on the bonding surface by selective etching of the high spots using, for example, standard photolithographic techniques; See Col. 5, Lns. 31-35).

Regarding claims 6 and 18, Tong discloses the bonding method and apparatus wherein the surface roughness process/control step is a method using atmospheric plasma (In a first example of the method according to the invention, the VSE process consists of a gas or mixed gas (such as oxygen, argon, nitrogen, CF.sub.4, NH.sub.3) plasma process at a specified power level for a specified time (FIG. 3C). Almost any gas or gas mixture that will not etch surface 34 excessively can be used for the room temperature bonding method according to the invention; See Col. 6, Lns. 9-11).

Regarding claims 7 and 19, Tong discloses the bonding method and apparatus wherein the surface roughness processing/control step is a blast treatment method wherein fine particles are blown (The plasma process may be conducted in different modes. Both reactive ion etch (RIE) and plasma modes may be used, as well as an inductively-coupled plasma mode (ICP). Sputtering may also be used; See Col. 5, Lns. 66-67, Col. 6, Lns. 1-2).

Regarding claim 8, Tong discloses the bonding method according to claim 1, wherein the surface-treatment step includes projecting energy particles or waves toward the bonding surfaces under the atmospheric pressure (The plasma process may be conducted in different modes. Both reactive ion etch (RIE) and plasma modes may be used, as well as an inductively-coupled plasma mode (ICP). Sputtering may also be used; See Col. 5, Lns. 66-67, Col. 6, Lns. 1-2).

Regarding claim 9, Tong discloses the bonding method according to claim 1, wherein the surface-treatment step is performed at the same time with the bonding step (The bonding immediately after the RIE process may use a special bonding fixture

allowing immediate in situ bonding of the etched wafers. A diagram of the fixture is shown in FIG. 7. In plasma chamber 75 are two wafers to be bonded 70 disposed on RF electrodes 76 and 77. A plasma is formed in zone 79 by the application of RF power to the electrodes via moveable vacuum RF power feedthrough 74 and by the introduction of an appropriate gas or gas mixture through gas feedthrough 73. Element 71 is a vacuum feedthrough for mechanical actuator (not shown) to retract retractable spacer 72. Chamber 75 is pumped down to a desired vacuum level via pumps (not shown) and chamber inlet 78. In the case where a post-VSE process or post cleaning process is also a dry process, as discussed above, the VSE and post-VSE or post-cleaning may be conducted in chamber 75. After the plasma treatment to conduct the VSE process, the mechanical spacers 72 are retracted by the mechanical actuator and the wafers 70 are moved into contact with to begin the bonding process. The bonded wafers are then moved from the chamber into ambient or into another vacuum chamber (not shown) and stored for a desired period to allow the bonding to propagate by a wafer handling system (not shown); See Col. 7, Lns. 31-54).

Regarding claims 11 and 21, Tong discloses the bonding method and apparatus wherein the surface-treatment step includes irradiation of substances generated by atmospheric plasma (The plasma process may be conducted in different modes. Both reactive ion etch (RIE) and plasma modes may be used, as well as an inductively-coupled plasma mode (ICP). Sputtering may also be used; See Col. 5, Lns. 66-67, Col. 6, Lns. 1-2).

Regarding claim 12, Tong discloses the bonding method according to claim 1, wherein the bonding step is performed at room temperature (Desired species on the surfaces will further preferably react with each other when they are in sufficiently close proximity allowing chemical bonding between surfaces 34 and 36 at low or room temperature that is enhanced by diffusion or dissociation and diffusion of the reacted desired species away from the bonding interface; See Col. 6, Lns. 24-30).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong in view of Hori et al. (U.S. Patent Application Publication No. 2004/0105155, from hereinafter "Hori"). The teachings of Tong have been discussed above.

Regarding claims 5 and 17, Tong fails to teach the bonding method and apparatus wherein the surface roughness process/control step performs transferring an uneven surface profile to one bonding surface using a tool formed with a profile having a predetermined roughness.

Hori teaches the bonding method and apparatus wherein the surface roughness process/control step performs transferring an uneven surface profile to one bonding surface using a tool formed with a profile having a predetermined roughness (Concretely, the surface of the substrate to be coated is kept horizontal, and a fluid

composition having a viscosity of from 100 to 1000 mPa*m is cast onto the substrate and spread to form thereon a layer having a predetermined thickness. Next, a mold having a predetermined protrusion-groove microstructure profile is pressed against the layer of the fluid composition and kept as such under a pressure of from 0.5 to 120 kg/cm^2 at a temperature of from 20 degrees C to 150 degrees C for 60 seconds to 60 minutes; See ¶ [0082], [0083]).

In view of the teaching of Hori, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the above method and apparatus to transfer an uneven surface profile because Hori performs this process at room temperature while manufacturing a microelectronic device on a substrate. Hori discloses similar surface treating and processing used in wafer bonding.

6. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tong in view of Kub et al. (U.S. Patent No. 6,153,495, from hereinafter “Kub”). The teachings of Tong have been discussed above.

Regarding claims 10 and 20, Tong fails to teach the bonding method and apparatus wherein the surface-treatment step includes ultraviolet irradiation.

Kub teaches the bonding method and apparatus wherein the surface-treatment step includes ultraviolet irradiation (Plasmas, UV, ozone, and laser irradiations may also be used to clean the surface prior to bonding; See Col. 6, Lns. 20-22).

In view of the teaching of Kub, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ ultraviolet irradiation as a means

of surface-treatment because Kub discloses a method for making semiconductor devices by low temperature direct bonding much in the same way Tong does.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. DiBernardo whose telephone number is (571)270-7436. The examiner can normally be reached on Monday through Friday from 8:30am to 6:00pm with alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lisa M. Caputo can be reached on (571)272-2388. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. J. D./
Examiner, Art Unit 4136

/Lisa M. Caputo/
Supervisory Patent Examiner, Art Unit 4136